

LATERAL-CURRENT-FLOW BIPOLAR TRANSISTOR WITH HIGH EMITTER PERIMETER/AREA RATIO

CROSS-REFERENCE TO RELATED APPLICATION

- This application claims priority to Italian Patent Application No.
- 5 TO2002A 001090 entitled "Lateral-Current-Flow Bipolar Transistor with High Emitter Perimeter/Area Ratio", filed on December 17, 2002, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

- 10 The present invention relates to a lateral-current-flow bipolar transistor with high emitter perimeter/area ratio.

Description of the Related Art

- As is known, bipolar transistors may be made with vertical or lateral current flow. In the first case (vertical current flow), it is frequently necessary to
- 15 use layers dedicated only to form some regions of the transistor. In this way, the transistor may be integrated in a smaller area. In the second case (lateral current flow), it is possible to save on the production of some dedicated layers or regions, but the area required for integration is wider, as may be noted from the comparison between Figures 1 to 4 regarding PNP transistors.

- 20 In detail, Figures 1 and 2 illustrate a vertical-current-flow PNP transistor formed in a body 1 and comprising an epitaxial layer 2 of N^- type accommodating a first buried layer 3, of P^+ type; a second buried layer 4, of N^+ type, on top of the first buried layer 3; an insulation region 5, of N^+ type and annular shape, extending from the surface of the body 1 as far as the second
- 25 buried layer 4 and surrounding an insulated region 6; a collector well 7, of P type,

inside the insulated region 6; a collector contact region 8, of P⁺ type and an annular shape, extending inside the collector well 6; a base well 10, of N type, extending inside the collector well 6 and surrounded by the collector-contact region 8; and an emitter region 11, of P⁺ type, inside the base well 10.

5 Figures 3 and 4 illustrate a lateral-current-flow PNP transistor formed in a body 20, comprising an epitaxial layer 21, of N⁻ type, accommodating a first buried layer 22, of P⁺ type; an insulation region 23, of P⁺ type and annular shape, extending from the surface of the body 20 as far as the first buried layer 22 and surrounding an insulated region 26; a second buried layer 24, of N⁺ type, on top of
10 the first buried layer 22 inside the insulated region 26; a deep base region 25, of N⁺ type and annular shape, extending inside the insulated region 26 as far as the second buried layer 24; a base well 27, of N type, surrounded by the deep base region 25 and, underneath, by the second buried layer 24; a collector region 28, of P⁺ type and annular shape, inside the base well 27; and an emitter region 29, of P⁺
15 type, surrounded by the collector region 28.

As may be noted from Figures 3 and 4, the electrical performance of the lateral-current-flow transistor is regulated mainly by the geometry of the collector region 28 and of the emitter region 29, which are annular and concentric. In particular, the current gain h_{FE} depends upon the distance between the collector
20 region 28 and the emitter region 29 and upon the charge of the base well 27, whereas the current that can be carried depends upon the facing area between the collector region 28 and the emitter region 29, which is proportional to the perimeter or circumference thereof.

As may be noted from the comparison between Figures 2 and 4, the
25 dimensions of a lateral-current-flow PNP transistor are significantly larger than those of a vertical-current-flow PNP transistor and increase considerably with the current.

BRIEF SUMMARY OF THE INVENTION

The aim of the present invention is to provide a lateral-current-flow bipolar transistor able to carry a greater amount of current than known solutions, without increasing significantly the surface area.

5 According to the present invention, there is provided a lateral-current-flow bipolar transistor, as defined in claim 1.

 In practice, the transistor comprises a base well with a first conductivity type, which accommodates conductive regions with a second conductivity type forming emitter and collector regions. One of the emitter and
10 collector regions comprises an internal conductive region and an external conductive region, wherein the external conductive region has an annular shape and the internal conductive region extends internally and at a distance from the external conductive region, and another of the emitter and collector regions comprises an intermediate conductive region, of an annular shape, which extends
15 between and at a distance from the internal and external conductive regions.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, an embodiment thereof is now described, purely by way of non-limiting example and with reference to the attached drawings, wherein:

20 Figure 1 illustrates a cross-section of a known vertical-current-flow PNP transistor;

 Figure 2 illustrates a top view of the transistor of Figure 1;

 Figure 3 illustrates a cross-section of a known lateral-current-flow PNP transistor;

25 Figure 4 illustrates a top view of the transistor of Figure 3;

 Figure 5 illustrates a cross-section of a lateral-current-flow PNP transistor, according to one embodiment of the present invention; and

 Figure 6 illustrates a top view of the transistor of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

Figures 5 and 6 illustrate an embodiment of a lateral-current-flow PNP transistor formed in a body 50 comprising a substrate 51, of N^+ type, and an epitaxial layer 52, of N^- type, formed by a bottom portion 52a and by a top portion 52b. A first buried layer 53, of P^+ type, extends between the bottom portion 52a and the top portion 52b of the epitaxial layer 52; an insulation region 54, of P^+ type and annular shape, extends from the surface of the body 50 as far as the first buried layer 53, and delimits, together with the latter, an insulated region 56. A second buried layer 55, of N^+ type, extends inside the insulated region 56 on top of and in contact with the first buried layer 53; a deep base region 57, of N^+ type and annular shape, extends inside the insulated region 56 as far as the second buried layer 55, and delimits, in the top portion 52b of the epitaxial layer 52, a base well 58. The base well 58 accommodates an external collector region 60, of P^+ type and annular shape; an emitter region 61, of P^+ type and annular shape, surrounded by the external collector region 60; and an internal collector region 62, of P^+ type and circular shape, surrounded by the emitter region 61.

An insulating layer 70 extends on top of the body 50 and accommodates metal contacts and connection lines, enabling electrical connection of the various regions; in particular, the collector regions 60, 62 are electrically connected to a same collector electrode C by a collector-connection region 64 comprising a portion 64b overlying the internal collector region 62; a portion 64c overlying the external collector region 60; and a connection portion 64a extending on top of the emitter region 61. In addition, the emitter region 61 is connected to an emitter electrode E through a C-shaped emitter-connection region 65 (represented hatched in Figure 6) to enable, in the open area, the passage of the connection portion 64a and the connection between the collector regions 60, 62. The collector-connection region 64 and the emitter-connection region 65 are formed in a same metal layer.

By virtue of the annular shape of the emitter region 61 and its intermediate arrangement between the two collector regions 60, 62, which enables the emitter region 61 to face the collector regions on both its internal and external circumferences, the emitter-collector facing area is considerably increased, without
5 this leading, on the other hand, to any significant increase in the total area. Thereby, the current injected from the internal circumference of the emitter region 61 is collected by the internal collector region 62 and sent, together with the current collected by the external collector region 60, to the collector electrode C through the contact region 64.

10 The process of fabrication of the PNP transistor of Figures 5 and 6 is described hereinafter.

On the substrate 51 with a high dopant concentration of N type a bottom portion 52a of the epitaxial layer 52 is grown. The concentration and thickness of the bottom portion 52a are chosen appropriately according to the
15 voltage levels required for operation of the finished device.

The first and second buried layers 53, 55 are then formed on the bottom portion 52a of the epitaxial layer, by ion implantation and a subsequent diffusion, the second buried layer 55 being made with a smaller area and set on top of the first buried layer 53.

20 Next, on top of the bottom portion 52a, a top portion 52b of the epitaxial layer 52 is grown; then, the insulation region 54 is formed in the top portion 52b of the epitaxial layer 52, by ion implantation and subsequent diffusion step, the insulation region 54 reaching the first buried layer 53 and delimiting, together with the latter, the insulated region 56. Next, the deep base region 57 is
25 formed once again by ion implantation and subsequent diffusion step; the deep base region 57 reaches the second buried layer 55 on its edge and delimits, in the top portion 52b of the epitaxial layer 52, the base well 58.

Next, the collector regions 60, 62 and the emitter region 61, of P⁺ type are formed by ion implantation, in a concentric way with respect to one

another. The electrical contacts, the electrical-connection regions, and the electrodes E, B, C associated to the different regions of the transistor, are formed on the front surface of the wafer 50, using photolithography and deposition techniques.

5 The bipolar transistor described above presents the following advantages.

 The formation of an annular-shaped emitter region 61 enables division of the collector region into internal and external portions (collector regions 62, 60), which are electrically connected in parallel by a metal connection region, and hence enables maximization of the facing area between emitter and collector, which now comprises both the external and the internal lateral surfaces of the emitter region. Consequently, the emitter current is higher than in a known PNP transistor thanks to the ratio between the total length of the respective circumferences (a total length which, for the emitter region 61, comprises both the internal and the external circumferences, as indicated in the figure).

 For a current of the same amplitude, the area of silicon occupied by the transistor according to the invention is much smaller in known PNP transistors.

 The described structure enables two PNP transistors to be obtained which have the same emitter and independent collectors, the currents thereof are in proportion to the internal circumference/external circumference of the emitter region. In this way, the so-called "matched transistors" solution is obtained, without, on the other hand, any need to design two transistors close to one another, which calls for more space.

 The structure described herein enables, as indicated, provision of two transistors with different values of h_{FE} . In fact, by setting each of the collector regions at an appropriate distance from the emitter region, thereby effectively adjusting the facing area between the emitter and each collector region, it is possible to obtain any combination of h_{FE} gains, with a considerable advantage in

space as compared to a traditional solution that uses two distinct transistors having different gains.

Finally, it is evident that modifications and variations may be made to the bipolar transistor described herein, without thereby departing from the scope of
5 the present invention.

For example, the same solution may be used for NPN transistors by reversing the conductivity type of the various regions, should the process envisage corresponding layers and steps, or by adding a single layer.

In addition, the exact shape of the different regions (emitter, collector,
10 insulation) may vary. Furthermore, if necessary, an additional emitter ring and an additional collector ring may be provided outside the regions 60-62.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit
15 and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.